PATENT
Docket No. **PTLIN-9801**

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of
Inventor(s): **Paul T. Lin**

WARNING: Patent must be applied for in the name(s) of all the actual inventor(s). 37 CFR 1.41(a) and 1.53(b).

For (title): SUBSTRATE ON CHIP (SOC) MULTIPLE-CHIP MODULE (MCM) WITH CHIP-SIZE –PACKAGE (CSP) READY CONFIGURATION

1. Type of Application

This new application is a(n) (check one applicable item below):

X Original
_ Design
_ Plant

WARNING: Do not use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. 371(c)(4) unless the International Application is being filed as a divisional, continuation or continuation-in part Application.

NOTE: If one of the following 3 items apply then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED.

_ Divisional
_ Continuation
_ Continuation-in-part (CIP)

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date **May 18, 1999** in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number **EJ136073926US** addressed to: Box Patent application, Assistant Commissioner for Patents, Washington, D.C. 20231.

Ching-lu Lin
(Type or print name of person mailing paper)

Ching-lu Lin
(Signature of person mailing paper)

NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon to mailing. 37 CFR 1.10(b).

2. Benefit of Prior U.S. Application(s) (35 USC 120)

NOTE: If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

_X_ The new application being transmitted claims the benefit of prior U.S. application(s) and enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed Which Are Required For Filing Date Under 37 CFR 1.53(b) (Regular) or CFR 1.153 (Design) Application

__16__ Pages of specification
__2__ Pages of claims
__1__ Pages of Abstract
__10__ Pages of Drawings
__X__ formal
__ informal

WARNING: DO NOT submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted the Office. **Only one copy is required or desired.** Comments on proposed new 37 CFR 1.84. Notice of March 9, 1988 (1990 O.G. 57-62).

NOTE: "Identify indicia such as the serial number, group and unit, title of the invention, attorney's docket number, inventor's name, number of sheets, etc., not to exceed 2 3/4 inches (7.0 cm.) in which may be placed in a centered location between the side edges within three fourths inch (19.1 mm.) of the top edge. Either this marking technique on the front of the drawing is acceptable." Proposed 37 CFR 1.84 (1). Notice of March 9, 1988 (1090 O.G. 57-62)

4. Additional papers enclosed

_ Preliminary amendment
_ Information Disclosure Statement
_ Form PTO-1449
_ Citations
_ Declaration of Biological Deposit
_ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
_ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
_ Special Comments
_ Other

5. Declaration or oath

X Enclosed

executed by (*check **all** applicable boxes*)

X inventor(s).

_ legal representative of inventor(s). 37 CFR 1.42 or 1.43

_ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached

_ this is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. *See item 13 below for fee.*

_ Not Enclosed.

WARNING: Where the filing is a completion in the U.S. of an International Application but where a declaration is not available or where the completion of the U.S. application contains subject matter in addition to the International Application the application may be treated as a continuation or continuation-in-part as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.

_ Application is made by a person authorized under 37 CFR 1.41 (c) on behalf of *all* the above named inventor(s). The declaration or oath, along with the surcharge required by 37 CFR 1.16 (e) can be filed subsequently.

NOTE: It is important that **all** the correct inventor(s) are named for filing under 37 CFR 1.41 (c) and 1.53 (b).

6. Inventorship Statement

WARNING: If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the **last** claimed invention was made, should be submitted.

The inventorship for all the claims in this application are:

X The same

or

_ Are not the same. An explanation, including the ownership of the various claims at the time the **last** claimed invention was made.

_ is submitted

_ will be submitted.

7. Language

NOTE: An application including a signed oath or declaration may be filed in a language other than English. A verified English translation of the non-English language application and the processing fee of $30.00 required by 37 CFR 1.17(k) is required to be filed with the application or within such time as may be set by the Office. 37 CFR 1.5(d).

NOTE: A non-English oath or declaration in the form provided or approved by the PTO need not be translated. 37 CFR 1.69(b).

X English

_ non-English

_ the attached translation is a verified translation. 37 CFR 1.52(d).

8. Assignment

_An assignment of the invention to _____

_is attached

_ will follow

NOTE: "If an assignment is submitted with a new application, send two separate letters-one for the application and one for the assignment" Notice of May 4, 1990.

9. Certified Copy

Certified cop(ies) of application(s)

_____

(country) (appl.no.) (filed)

from which priority is claimed

_ is (are) attached . A separate "ASSIGNMENT COVER LETTER ACCOMPANYING NEW PATENT APPLICATION" is also attached

_ will follow.

NOTE: The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37CFR 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35USC120 is itself entitled to priority from a prior foreign application then complete item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10 Fee Calculation (37 CFR 1.16)

A X Regular application

CLAIMS AS FILED				
Number filed	Number Extra		Rate	Basic Fee $790.00
Total Claims 37 CFR 1.16(c)	6-20 = 0	x	$22.00	0.00
Independent Claims (37CFR 1.16(b))	1 -3 = 0	x	$ 82.00	0.00
Multiple dependent claim(s), if any (37 CFR 1.16(d))			$270.00	0.00

_ Amendment Cancelling extra claims enclosed.

_ Amendment deleting multiple-dependencies enclosed.

_ Fee for extra claims is not being paid at this time.

note: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37CFR1.16(d).

Filing fee calculation $ 790.00

B. _ **Design application**
($310.00 - 37 CFR 1.16(f))

Filing fee calculation $_____

C _ **Plant application**
($510.00 - 37 CFR 1.16(g))

Filing fee calculation $_____

11. Small Entity Statement(s)

_X Verified Statement(s) that his is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

Filing Fee Calculation (50% of **A, B,** or **C** above) $ 395.00

NOTE: any excess of the full fee paid will be refunded if a verified statement and a refund request are filed within 2 months of the date of timely payment of a full fee. 37 CFR 1.28(a).

12. Request for International-Type Search (37 CFR 1.104(d)) (*complete, if applicable*)

_ Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made At This Time

_ Not Enclosed

_ No filing fee is to paid at this time. (*This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.*)

X Enclosed

X basic filing fee	$ 395.00
__ recording assignment ($40.00; 37 CFR 1.21(h))	$ 0.00
_petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached. ($120.00; 37 CFR 1.47 and 1.17(h))	$
_ for processing an application with a specification in a non-English language. ($300.00; 37 CFR 1.52(d) and 1.17(k))	$
_ processing and retention fee ($130.00; 37 CFR 1.53(d) and 1.21(l))	
_ fee for international-type search report ($40.00; 37 CFR 1.21(e))	$

NOTE: 37 CFR 1.21(l) establishes a fee for processing and retaining any application which is abandoned for failing to complete the application pursuant to 37 CFR 1.53(d) and this, as well as the changes to 37 CFR 1.53 and 1.78, indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid or the processing and retention fee of 1.21(l) must be paid within 1 year from notification under 53(d).

Total fees enclosed $ 395.00

14. Method of Payment of Fees

X Check in the amount of $ 395.00

_ Charge Account No. in the amount of $_____. A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner the it is clear for which purpose the fees are paid. 37 CFR 1.22(b).

15. Authorization to Charge Additional Fees

WARNING: if no fees are to be paid on filing the following items should **not** be completed.

WARNING: Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.

X The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 120005.

X 37 CFR 1.16(a), (f) or (g) (filing fees)

X 37 CFR 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 CFR 1.16(d)) it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

_ 37 CFR 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later then the filing date of the application)

_ 37 CFR 1.17 (application processing fees)

WARNING: While 37 CFR 1.17(a),(b) (c) and (d) deal with extensions of time under 1.136(a) this authorization should be made only with the knowledge that: "Submission of the appropriate extension fee under 37 C.F.R. 1.136(a) is to avail unless a request or petition for extension is filed." (Emphasis added). Notice of November 5, 1985 (1060 O.G. 27)

_ 37 CFR 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 CFR 1.311(b))

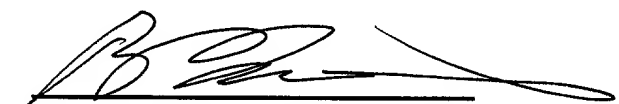
NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 CFR 1.311(b).

NOTE: 37 CFR 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application...prior to paying, issue fee". From the wording of 37 CFR 1.28(b): (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

16. Instructions As to Overpayment

_ credit Account No.

X refund



Reg. No.33,948 **SIGNATURE OF ATTORNEY**

Bo-In Lin

Tel. No. (650) 949-0418 Type or print name of attorney

P.O. Address : **13445 Mandoli Drive,**
Los Altos Hills, CA 94022

X **Incorporation by reference of added pages**

Check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR A NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED

X Plus Added Pages For New Application Transmittal Where Benefit Of Prior U.S. Application(s) Claimed

Number of pages added 1

_ Plus Added Pages For Papers Referred To In Item 4 Above

Number of pages added _____

_ Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added _____

__ **Statement Where No Further Pages Added**

(If no further pages form a part of this Transmittal then end this Transmittal with this page and check the following item)

__ This transmittal ends with this page

SUBSTRATE ON CHIP (SOC) MULTIPLE-CHIP MODULE (MCM) WITH CHIP-SIZE –PACKAGE (CSP) READY CONFIGURATION

This Application claims a Priority Date of June 1, 1998, benefited from a previously filed Provisional Application 60/087,604 filed on June 1, 1998 by a same Inventor of this Patent Application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the electronic package. More particularly, this invention relates to a novel technique to simplify the manufacture process for a substrate of memory chip module with chip layout placing the bonding pads in the center portion of the chip. Furthermore, the substrate-on-chip chip modules are assembled as CSP-ready multiple-chip-module (MCM) packaging configuration. The assembling and testing processes of this CSP ready MCM are simplified to achieve a lower production cost. Furthermore, the procedures to repackage and utilize the know-good-die (KGD) packaged as a known-good-CSP (KGCSP) after testing is also simplified such that an effective method is provided to minimize the wastes of the known -good-dice.

2. Description of the Prior Art

There is a concern in applying the surface mount technology (SMT) to electronic package that package cracking, e.g., a pop corning phenomenon, may occur upon board mounting. This is generally caused by permeation of moisture through the plastic package body. In order to prevent this pop-corning phenomenon, very stringent requirements are imposed for SMT package design, materials, processes, dry packing, and qualification tests to prevent package cracks and to assure package reliability. Fig. 5 shows an example of such requirements for a SMT package. Time for production and costs are

increased due to processes taken to satisfy these requirements. Examples of such packages are disclosed as that in U.S. Patent 5,684,330, where the entire packaging structure is encapsulated with plastic molding. This type of packaging configuration is also implemented for most of the dynamic ransom access memory (DRAM) chips where the bonding pads are placed in the central portion of the chip. For the purposes of improving electrical performance and minimizing packaging width, a lead-on-chip (LOC) technology is applied. Each individual package is tested and burned in and good packages are then surface mounted on a module substrate in DIMM or PCMCIA format with edge connectors for socket applications. Examples of electronic packages are disclosed in U.S. Patents 5,346,861 by Khandros et al., 5,068,712 by Murakami et al., and 4,862,245 by Pashby et al. As plastic molding of the entire structure is shown for these patented packaging assemblies, the difficulties of applying more elaborate stringent requirements for assembling and testing the packages are not resolved by these patented package configurations.

Furthermore, there is a different challenge faced by those applying the multiple-chip-module (MCM) technology to package multiple electronic chips into a single module. This challenge arises from the fact that a MCM module can function properly only if every chip assembled into this MCM package is individually a good die. Also, due to the accumulative effect, even a small percentage of reject rate for the individual chips, an unacceptable loss to the MCM packages is generated in using these chips. For example, a 99% chip acceptance rate for the individual chips, when assembled into eight-chip modules (X8 modules) as dual in-line memory module (DIMM) or single-in-line-memory module (SIMM) packages, an 8% loss or rework rate is generated which is clearly unacceptable.

In order to reduce wastes of resources committed to packaging chips which are not good dice, burn-in tests of individual chips are performed again after a wafer probe operation to identify the known good dice (KGD) before a MCM packaging processes are carried out.

However, the processes for burning-in each individual chip or chip-size package (CSP) are very expensive due to the requirements of special testing sockets, and large dedicated burn-in board. Furthermore, difficult handling techniques are required to test these individual chips. Due to these special and expensive requirements for qualifying an integrated circuit (IC) chip as a known good die (KGD), it generally costs more to test a chip than to test a package. For the same reasons, the price of a known good die is approximately two to three times as that of a untested die. Even with the high cost of testing and a much higher price to use the KGD, due to the concern of accumulative losses when chips are assembled as multiple chip modules, there is no choice but to employ the KGDs.

In addition to the costs related to the requirement of using the chip size packages, two level of substrates or lead frames are employed in conventional multiple chip modules wherein known good dice contained in a CSP are assembled. The first level of substrate is used for packaging individual chips. The multiple chip module substrate is a second level substrate, which is used for mounting multiple chips each packaged in a CSP module. Additional costs are incurred in this two level substrate structure since it requires more material and processing. This two-level substrate structure further presents another disadvantage that the packages have a higher profile and higher thermal resistance causing poor heat dissipation. In order to enhance device miniaturization, more and more modern applications implemented with packaged electronic chips require a reduced thickness. Conventional MCM packages implemented with a two-level substrate structure have very limited usefulness in modern miniaturized devices when an electronic packages with a very small thickness are required.

Therefore, a need still exits in the art to provide an improved configuration and procedure for testing and packaging the multiple chip modules to reduce the cost of testing. The need also exists for a new configuration to more conveniently and economically reuse the known good dice when a known good die is packaged with other failed

chips into a multiple-chip-module. There is further a need to provide an improved packaging configuration, particularly for the SMT packages with pop-corning difficulties, such that the packaging and testing requirements can be relaxed to shorten the production time and reduce the production costs without degrading the product reliability.

SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide an improved packaging configuration to relax the manufacturing and testing requirements for the SMT electronic packages for individual IC dice. The IC chips are then assembled as an improved multiple chip modules (MCMs) to reduce the cost of testing and to more conveniently and economically save and reuse the known good dice after the testing. The improved chip module packages and the MCM assembly are provided to overcome the aforementioned difficulties and limitations encountered in the prior art.

Specifically, it is an object of the present invention to provide an improved chip module for surface mounting to an improved MCM assembly. The improved chip module is attached via an adhesive layer to the backside of a laminated board provided with a bonding wire opening and bonding pads on the top surface. The chip is then wire bonded to the board with bonding wires pass through the bonding wire opening. The chip module, i.e., a substrate on chip (SOC) module, is further configured as a chip-size package (CSP) ready assembly with via connectors penetrating the laminating board interconnecting the bonding pads to an array of solder balls to be placed on MCM assembly as a CSP.

Another object of the present invention is to provide an improved chip module for surface mounting to an improved MCM assembly. The encapsulation for the improved chip module is only required to cover the bonding wire opening for protecting the bonding

wires such that the packaging procedures are simplified and the criteria for assembly and testing the package are significantly relaxed.

Another object of the present invention is to provide an improved chip module for surface mounting to an improved MCM assembly. The heat dissipation for the improved chip module is significantly improved because the entire back surface of the chip module is exposed for direct heat dissipation. Further improvement of heat dissipation is achieved by attaching the active IC surface to a single core metal of a long DIMM substrate for spreading the heat.

Another object of the present invention is to provide an improved MCM configuration and procedure for testing and packaging multiple chips as MCM assemblies. A CSP ready MCM board is employed wherein a plurality of CSP contact terminals are provided with CSP-ready via connectors penetrating the MCM board such that the probed good dice (PGD) packaged in SOC modules when assembled in a failed MCM can be conveniently separated and easily reused. These tasks can be accomplished without complicated and time consuming rework processes whereby the total production cost can be significantly reduced.

Another object of the present invention is to provide an improved MCM configuration and procedure for testing and packaging multiple chips as MCM assemblies by employing a CSP ready MCM board. A plurality of CSP contact terminals are provided with CSP-ready via connectors penetrating the MCM board such that the improved CSP-ready MCM board can be applied for different kinds of integrated circuit chips including flip-chips, wire-boding chips, and other types of chips. The novel CSP-ready reusable MCM board can be broadly applied to assemble various kind of electronic packages.

Another object of the present invention is to provide an improved MCM configuration and procedure for testing and packaging multiple chips as MCM assemblies by mounting multiple chips directly

on a CSP-ready MCM board. Only a single level of substrate is required for majority of MCM assemblies, which pass the burn-in and functional tests such that the height of the package profile of the MCM assembly can be reduced.

Briefly, in a preferred embodiment, the present invention includes an integrated multiple-substrate-on-chip-module (MSOCM) assembly. This assembly includes a chip-size package (CSP)-ready MSOCM board having a top surface and a bottom surface. The CSP-ready MCM board includes a plurality of bonding-wire windows and the bottom surface further includes a plurality of board bonding-pads near the bonding-wire window. The assembly further includes an adhesive layer disposed on top of the CSP-ready MCM board having also having a plurality of bonding wire windows corresponding to and aligned with the bonding wire windows on the MCM board. The assembly further includes a plurality of integrated circuit (IC) chips mounted onto the adhesive layer over the top surface of the CSP-ready MCM board. Each of the IC chips is provided with a plurality of chip bonding pads facing an open space defined by the bonding wire windows. The assembly further includes a plurality of bonding wires disposed in the space defined by the bonding-wire windows and interconnected between each of the chip bonding pads and a corresponding board bonding pad disposed on the bottom surface of the CSP-ready MSOCM board.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment which is illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are cross sectional views of a chip memory module and multiple modules on an integrated printed-circuit board

respectively of this invention provided with improved packaging configuration;

Fig. 1C is a cross sectional view of another substrate on chip (SOC) module of this invention;

Fig. 1D is a cross sectional view of another substrate on chip (SOC) module with improved heat dissipation performance of this invention;

Fig. 2A shows the cross sectional view for a multiple chip module assembly of SOC modules supported on a CSP-ready MCM board of this invention;

Fig. 2B shows a cross sectional view of a known good SOC module separated from the MCM assembly of Fig. 2A after the burn-in tests and repackaged as a known good CSP chip according to the configuration of this invention;

Fig. 2C shows a cross sectional view of a repaired MCM assembly with a known-good replacement SOC module attached at the bottom surface of the CSP-ready MCM board;

Fig. 3A shows top view of a CSP-ready MCM board which are provided with a plurality of standard edge testing pins for conducting both the burn-in and functional tests employing standard testing sockets;

Fig. 3B shows a configuration of the MCM board with edge testing pins inserted into a standard testing socket for carrying out burn-in and functional tests directly on the MCM board;

Figs. 4A and 4B are two flow charts showing the processing steps employed by a conventional MCM packaging and testing method in comparison to a simplified method used by the MCM assembly mounted on a CSP-ready MCM board of this invention; and

Fig. 5 shows the processing steps implemented to satisfy the testing requirements of a conventional packaging configuration.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to Fig. 1A for a cross sectional view of a substrate-on-chip (SOC) memory module 120 of this invention. The SOC memory module 120 includes an integrated circuit (IC) chip 101, e.g., a memory chip with a central pads layout having the bonding pads placed near the center-portion of the chip. The memory chip 101 is attached to a laminated printed circuit board 103 via an adhesive layer 102. The laminated PCB 103 has a bonding-wire window 104 opened at the bottom layers provided for allowing a plurality of bonding wires 104' to pass through for interconnecting the bonding pads 101' on the memory chip 101 to corresponding bonding pads 103'. The multiple-layer laminated PCB 103 further includes a cavity 104' opened from the top layers of the PCB 103 on top of the bonding wire window 104. The cavity 104' is opened with slightly greater area than the bonding wire window 104 thus exposed the top surface of the bottom layers. The bonding pads 103' are placed on the exposed top surface of the bottom layers of the laminated PCB 103 exposed by the cavity 104". A plurality of metal traces 105 interconnect the substrate bonding pads 103' to a corresponding via connector 106 penetrating through the laminated PCB 103. Each of the via connector 106 is then connected to a corresponding solder balls 130. The multiple-layered laminated PCB 103 further includes built-in passive components 107 such as capacitors, resistors, or inductors depending on various requirements of specific circuit design. The cavity 104" and the bonding wire window 104 opened for wire bonding connections between the IC chip 101 and the circuit elements on the substrate 103 is then encapsulated. An encapsulation layer 108 is employed to seal and protect the IC chip 101 and the bonding-wires 104'. The SOC module 120 has a special advantage that the backside 101" of the IC chip 101 is totally exposed for direct heat dissipation. The thermal performance of the IC chip and the package is significantly improved.

Fig. 1B shows another cross sectional view of multiple SOC modules of Fig. 1A manufactured and mounted on an integrated multiple-layered laminated PCB 103". The integrated PCB 103" has separation lines 109 provided between each individual SOC module. In stead of the solder balls as that shown in Fig. 1A, each of these individual-SOC modules is now provided with a land grid array 130'-1, 130'-2 and 130'-3. This assembly of multiple SOC modules mounted on an integrated PCB board 103" provided with separation lines can be implemented as a composite flip chip. This assembly as shown constitutes a CSP-ready multiple-chip-module (MCM) package. Providing these separation lines between the individual SOC modules achieves special advantages where each SOC module can be converted as a CSP chip as will be further described below.

The exact design and material of SOC 102 will depend of the particular layout of pad locations and the heat dissipation requirements. For the lowest cost approach, an industry-standards FR4 glass-epoxy laminate is employed. Because it has a relatively low Tg in 110°C to 130°C, high ultrasonic waves together with low temperature-thermal-compression-bonding below 120°C must be applied. Also, the encapsulation curing temperature has to be kept below the temperature of Tg. In the case that high heat dissipation is required, metal core laminated substrate such as ViperBGATM by Prolinx can be used. Obviously, the standard ball-grid-array (BGA) substrate of bismaleimide triazine (BT) resin laminate can also be employed. The width of the bonding wire opening will be very narrow in the range of 20 to 60 mils and the length is fairly long which is in the range of 150 to 300 mils depending on the die size. Double-sided adhesive of either thermal plastic or epoxy can be used to attach substrate to the front of memory device. Alignment of the dice will be required so that all centrally located bond pads will be exposed through the substrate window for subsequent wire bonding operation. The chip-size-package ready module substrate can also be built with integrated thin film passive components 107 such as capacitors and or resistor into a multiple layer

structure to further reduce the size and improve the electrical performance of the memory module.

Fig. 1C is a cross sectional view of another preferred embodiment of an SOC module 120' which is basically identically structured as the SOC module 120 shown in Fig. 1A. The only differences are first; the PCB laminated substrate 103" of this preferred embodiment is a single layer PCB board. There are no built-in passive components provided on several layers as that shown in Figs. 1A and 1B above. Secondly, other than the bonding wire window 104, there is no separate cavity opened from the top as that of the multiple-layer laminated PCB board 103. Thirdly, the encapsulation 108' of this embodiment is a liquid encapsulation provided with encapsulation dam 108". This single layered SOC module has a special advantage that the manufacture processes are further simplified to achieve lower production costs. The lower cost is achieved by depositing the encapsulation material as a liquid drop in each cavity. The liquid encapsulation is then solidified after a curing process.

Fig. 1D is another preferred embodiment of an SOC module 200, which has improved thermal dissipation. The structure of this SOC module is similar to that shown in Figs. 1A and 1C except that the substrate 203 is a metal core substrate. The IC chip is attached to the metal core substrate 203 via a low modules adhesive layer 202. The metal core substrate 203 has a window 204 for passing the bonding wires 204' there through. The cavity 204 is also padded with a dielectric or anodized layer 202'. The bonding wires 204' are electrically connected to interconnection metal traces 205 then connected to solder balls 230 separated by solder masks 206. The solder masks 206 provide special advantages that solder bridging is prevented and electric isolation of the solder balls 230 are improved. The SOC module is especially suitable for DIMM when higher heat dissipation rate is required. In addition to the advantage that the backside of the IC chip 201 is totally exposed for dissipating heat, the metal core substrate 203 further provides an excellent heat-conducting path. Heat generated

from the IC chip 201 is conducted through the meal core substrate 203 to the solder balls 230. Higher heat dissipating rates are therefore achieved. The metal core substrate further includes prescribed separation lines 209 provided with a ridge opening 209' along each of the separation lines 209 such that each SOC module may be conveniently separated.

Figs. 2A shows the cross sectional view of a multiple chip module 300 which includes multiple SOC modules, e.g., 320-1 to 320-3 as shown, supported on a CSP-ready MCM board 310, i.e., an integrated and ready-separable PCB, of this invention. This CSP ready MCM board is provided with a bonding wire cavity 104 for each SOC module. Similar to an SOC module shown in Fig. 1A except that the solder balls 130 are now replaced with a land-grid array. In addition, there are a plurality of conductive traces 105 for connecting between the circuit elements of other chips of multiple SOC modules, e.g., 320-1 to 320-3, etc. The CSP-ready MCM board 310 further includes a plurality of separation lines 109 between each SOC module.

By mounting these SOC modules 320-1 to 320-3 on this CSP-ready MCM board 310, the burn-in and testing processes can be performed directly on this MCM assembly 300 to determine if this MCM assembly 300, by packaging and connecting these SOC modules, is a good MCM assembly. If it is, then the whole MCM assembly 300 can be shipped out as a finished product. If one or several of these chips of the SOC modules are determined as unacceptable during the burn-in and testing processes, the MCM assembly is not useful in this MCM packaged form. However, several of the multiple SOC modules would have been identified as containing a known good die (KGD) after completion of the burn-in and testing processes. These SOC modules identified as containing a known good die can be separated from the CSP ready MCM board 310 by cutting them off from the separation lines 109. Referring to Fig. 2B, assuming that the SOC module 320-2 is identified as having a known good die, this SOC module 320-2 can be separated as an individual chip size package (CSP) 320-2'. This is

accomplished by forming a solder-ball array 130 connecting to each of the CSP-ready land-grid-array 130′ on the bottom surface provided in a cutoff section 109 of the CSP-ready MCM board 310 previously employed for supporting and packaging the MCM assembly 200. Each of these known good CSP chips, e.g., CSP chip 320-2′, has exposed edge traces 325′ which are used to interconnect multiple chips but are now cutoff to form this individual known good CSP chip 320-2′ for reuse.

According to Figs. 2A to 2B and above descriptions, the present invention discloses a chip-size package (CSP) ready multiple SOC module (MCM) board 310 having a top surface and a bottom surface for mounting and packaging a plurality of SOC modules 120-1 to 120-3 on the top surface. The MCM board is provided with a plurality of bonding wire windows for each of the SOC modules.

Fig. 2C shows an alternate method to repair a failed MCM assembly when one or more than one chips have failed in the burn-in or determined to be unacceptable after completion of the product acceptance tests. Suppose the SOC-module chip 120-2 is determined to be an unacceptable chip, an SOC-module flip chip 120-2″ which is a known good die is attached to the bottom of the MCM board 110 to replaced the known-bad-die (KBD) 120-2. The CSP-ready connection terminals 140 disposed on the bottom surface of the CSP-ready MCM board 110 is formed to have identical footprint and in mirror image to a CSP chip or a flip chip for the known bad die. The CSP-ready connection terminals are ready for connection to a replacement chip 120-2″ which is preferably an SOC-module flip chip as that shown in Fig. 1A or 1C.

Referring to Fig. 3A for top view of a CSP-ready MCM board 300 with a plurality of test pins 310 disposed on a testing insertion edge 305. There are multiple chips 315 mounted on this MCM board 300 and a plurality of conductive traces (not shown) connecting the chip connection terminals disposed on the board to the testing pins 310. There are two kinds of test pins among the test pins 310. The first kind of test pins are burn-in test pins 310-1 for connecting to a set of burn-in

socket receptors disposed in a standard socket (see Fig. 3B) for conducting a burn-in test. The second kind of test pins are board-level test pins 310-2 for connecting to a set of board-level socket receptors disposed in the standard socket shown in Fig. 3B for conducting a board-level test. Unlike the testing procedures employed in the conventional MCM assembly, the burn-in tests and the board-level tests for the MCM assembly 300 are now carried out directly on the board and using a single standard testing socket as that shown in Fig. 3B below. The procedures are much simplified compared to the conventional processes where the burn-in tests are performed for each individual chip by using special sockets which can endure higher temperatures used for burn-in tests, then the board-level tests are applied when all the chips are mounted on the MCM board. Referring to Fig. 3B, the MCM board 300 is inserted into a standard testing socket 350 for performing a burn-in test and a board level test. The standard burn-in and board-level testing socket 350 is made of materials, which can sustain a burn-in test temperature ranging from 100 to 150° C. This standard burn-in and board-level testing socket 350 includes two types of socket receptors 360, namely the burn-in socket receptors 360-1 and board-level socket receptors 360-2, for receiving the burn-in test pins 310-1 and the board-level test pins 310-2 respectively. Again, the testing socket 350 is also novel from a conventional board-level test socket. The conventional board-level test sockets are only provided with board level test socket adapters to receive board level test pins. In contrast, the burn-in and board-level testing socket 350 includes a set of socket adapters 360-1 to receive a set of burn-in test pins 310-1 and another set of socket adapters 360-2 to receive a set of board level test pins 310-2. Furthermore, the burn-in and board-level test socket 350 are made with material to sustain a higher burn-in test temperature which is not required in a conventional MCM board test socket.

By employing a CSP-ready MCM board and conducting the burn-in and board level tests directly with the multiple chips mounted on the board as described above, the process flow is significantly simplified. A comparison of these different process flows used by a

conventional MCM technique and that of a reusable CSP/MCM are listed in Figs. 4A and 4B respectively as two flow charts in parallel. The flow charts illustrate the processing steps at different stages including a wafer stage, a chip package stage, a chip package testing stage, a board testing stage, and a final shipment/rework/reject stage. In Fig. 4A, the processes begin (step 400') by receiving the wafer from front-end integrated circuit manufacture facility (step 410'). A wafer-bumping step is carried out (step 415') followed by a flip chip (step 420') or TAB (step 425') processes to complete the wafer level preparation works. Otherwise, if it is a wire bond type of chips, a wire bonding process (step 430) is carried out to complete the wafer level preparation works. An assembly and packaging process is performed (step 431') followed by a package testing (step 432') which generally include the burn-in tests for the packaged chips to assure good dice are identified for further multiple chip mounting and testing processes. Bad packages of individual IC chips are identified and rejected (step 433'). The good packages are selected for board mounting (step 434'). A board level testing process is performed (step 450') to identify the MCM assembly which has all good chip packages on board (step 451') and ready for shipment (step 455'). Or, the bad units identified are reworked (step 452') to obtain a completely acceptable MCM assembly for shipment (step 455').

Comparing to the conventional method, Fig. 4B shows a much more simplified processing flow. After the wafer level of works, i.e., steps 400 to steps 430, are completed, the individual chips are directly mounted to a CSP-ready MCM board of this invention by a direct chip attachment method (step 440). A combined burn-in and board level testing process is performed (step 450). If there are bad chips identified, the identified known bad chips can be replaced by a back-side replacement chip attachment method as that described above to repair the MCM assembly for shipment as a good package (step 470). Or, the identified good units are singluated (step 460) and repackaged as a known good CSP and ready for subsequent board mounting (step 440) and the bad chip units are rejected (step 480).

According to Figs. 1A to 4C, this invention discloses an integrated multiple-substrate-on-chip-module (MSOCM) assembly. This assembly includes a chip-size package (CSP)-ready MSOCM board 103 having a top surface and a bottom surface. The CSP-ready MCM board 103 includes a plurality of bonding-wire windows 104 and the bottom surface further includes a plurality of board bonding-pads 103′ near the bonding-wire window. The assembly further includes an adhesive layer 102 disposed on top of the CSP-ready MCM board 103 having also having a plurality of bonding wire windows corresponding to and aligned with the bonding wire windows on the MCM board. The assembly further includes a plurality of integrated circuit (IC) chips 101 mounted onto the adhesive layer 102 over the top surface of the CSP-ready MCM board 103. Each of the IC chips 101 is provided with a plurality of chip bonding pads 101′ facing an open space defined by the bonding wire windows 104. The assembly further includes a plurality of bonding wires 104′ disposed in the space defined by the bonding-wire windows 104 and interconnected between each of the chip bonding pads 101′ and a corresponding board bonding pad 103′ disposed on the bottom surface of the CSP-ready MSOCM board 103.

In a preferred embodiment, the CSP-ready MSOCM board 103 and the adhesive layer 102 further include a plurality CSP-ready separation lines 109 dividing each of the SOC modules mounted thereon. In a preferred embodiment, the CSP-ready MSOCM board 103 further includes a plurality of via connectors 106 penetrating the CSP-ready MSOCM board 103 and in electrical connection with a plurality of the board bonding pads 103′ via metal traces 105 disposed on the top surface of the MSOCM board 103. Each of the via connectors 106 further being in electric connection with a land grid array 130′ disposed on the bottom surface of the MSOCM board 103. In a preferred embodiment, the land grid array 130′ comprising a plurality of CSP-ready connection solder pads insulated by a plurality of solder masks. In a preferred embodiment, the MSOCM assembly further includes a plurality of solder balls 130 mounted on a plurality of the CSP-ready solder pads 130′ on the bottom surface of the CSP ready MSOCM board

103. In another preferred embodiment, the MSOCM assembly further includes a plurality of testing pins including a set of burn-in test pins and a set of board level test pins disposed on an edge of the CSP-ready MSOCM board 103 provided for conducting a plurality of burn-in and board level tests.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alternations and modifications will no doubt become apparent to those skilled in the art after reading the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alternations and modifications as fall within the true spirit and scope of the invention.

CLAIMS

I claim:

1. An integrated multiple-substrate-on-chip-module (MSOCM) assembly comprising:

a chip-size package (CSP)-ready MSOCM board having a top surface and a bottom surface, said CSP-ready MCM board includes a plurality of bonding-wire windows and said top surface further includes a plurality of board bonding-pads near said bonding-wire window;

an adhesive layer disposed beneath said CSP-ready MCM board having also having a plurality of bonding wire windows corresponding to and aligned with said bonding wire windows on said MCM board;

a plurality of integrated circuit (IC) chips mounted onto said adhesive layer under said bottom surface of said CSP-ready MCM board with each of said IC chips provided with a plurality of chip bonding pads facing an open space defined by said bonding wire windows; and

a plurality of bonding wires disposed in said space defined by said bonding-wire windows and interconnected between each of said chip bonding pads and a corresponding board bonding pad disposed on said top surface of said CSP-ready MCM board.

2. The MSOCM assembly of claim 1 further comprising:

said CSP-ready MSOCM board and said adhesive layer further include a plurality CSP-ready separation lines dividing each said IC chips mounted thereon.

3. The MSOCM assembly of claim 1 wherein:

said CSP-ready MSOCM board further includes a plurality of via connectors penetrating said CSP-ready MSOCM board and in electrical connection with a plurality of said chip bonding pads via metal traces disposed on said bottom surface of said MSOCM board; and

each of said via connectors further being in electric connection with a land grid array disposed on said top surface of said MSOCM board.

4. The MSOCM assembly of claim 4 wherein:

said land grid array comprising a plurality of CSP-ready connection solder pads insulated by a plurality of solder masks.

5. The MSOCM assembly of claim 1 further comprising:

a plurality of solder balls mounted on a plurality of said CSP-ready solder pads on said top surface of said CSP ready MSOCM board.

6. The MSOCM assembly of claim 1 further comprising:

a plurality of testing pins including a set of burn-in test pins and a set of board level test pins disposed on an edge of said CSP-ready MCM board provided for conducting a plurality of burn-in and board level tests.

ABSTRACT

. The present invention includes an integrated multiple-substrate-on-chip-module (MSOCM) assembly. This assembly includes a chip-size package (CSP)-ready MSOCM board having a top surface and a bottom surface. The CSP-ready MCM board includes a plurality of bonding-wire windows and the bottom surface further includes a plurality of board bonding-pads near the bonding-wire window. The assembly further includes an adhesive layer disposed on top of the CSP-ready MCM board having also having a plurality of bonding wire windows corresponding to and aligned with the bonding wire windows on the MCM board. The assembly further includes a plurality of integrated circuit (IC) chips mounted onto the adhesive layer over the top surface of the CSP-ready MCM board. Each of the IC chips is provided with a plurality of chip bonding pads facing an open space defined by the bonding wire windows. The assembly further includes a plurality of bonding wires disposed in the space defined by the bonding-wire windows and interconnected between each of the chip bonding pads and a corresponding board bonding pad disposed on the bottom surface of the CSP-ready MSOCM board.

Fig. 1A

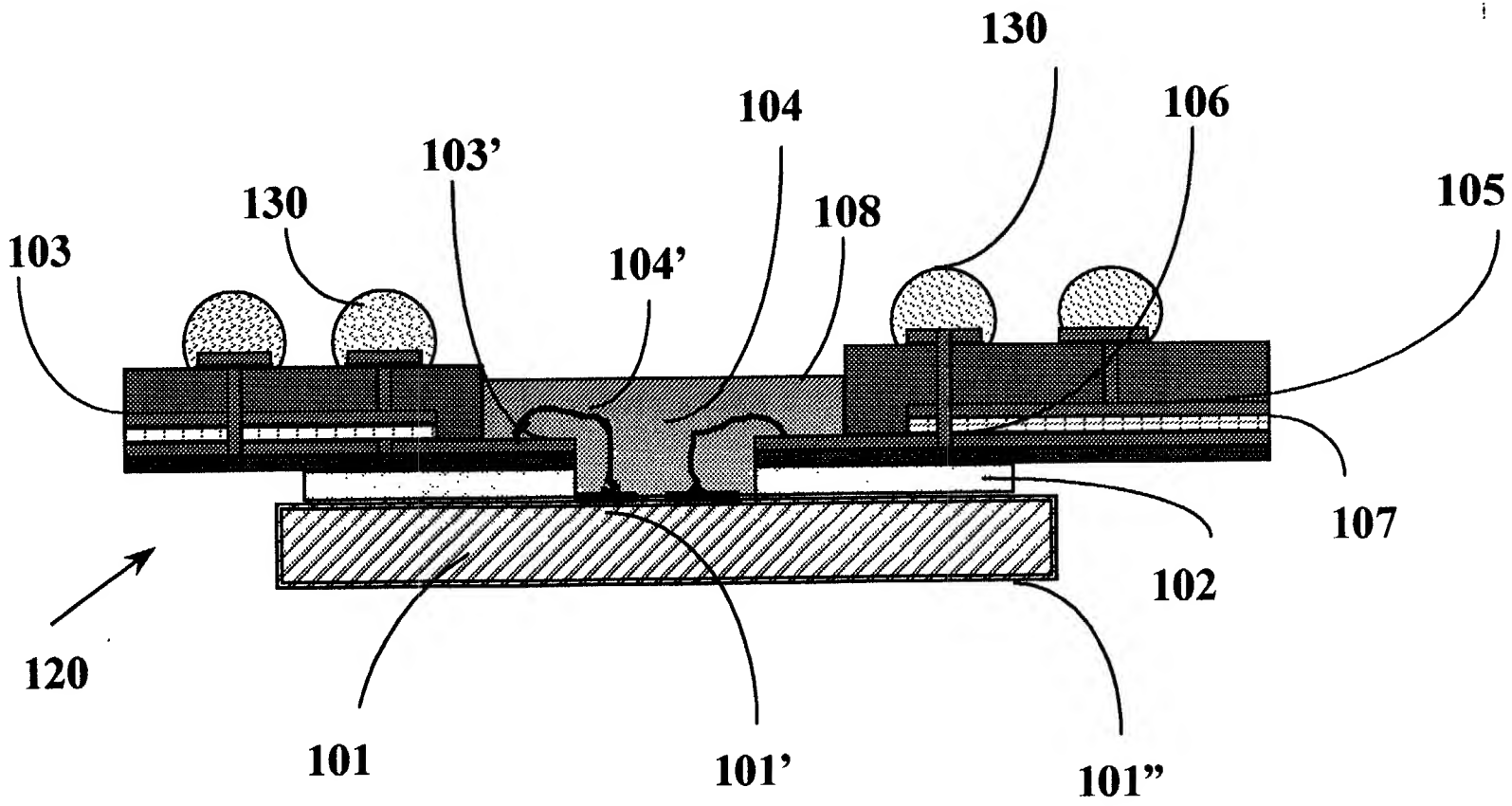
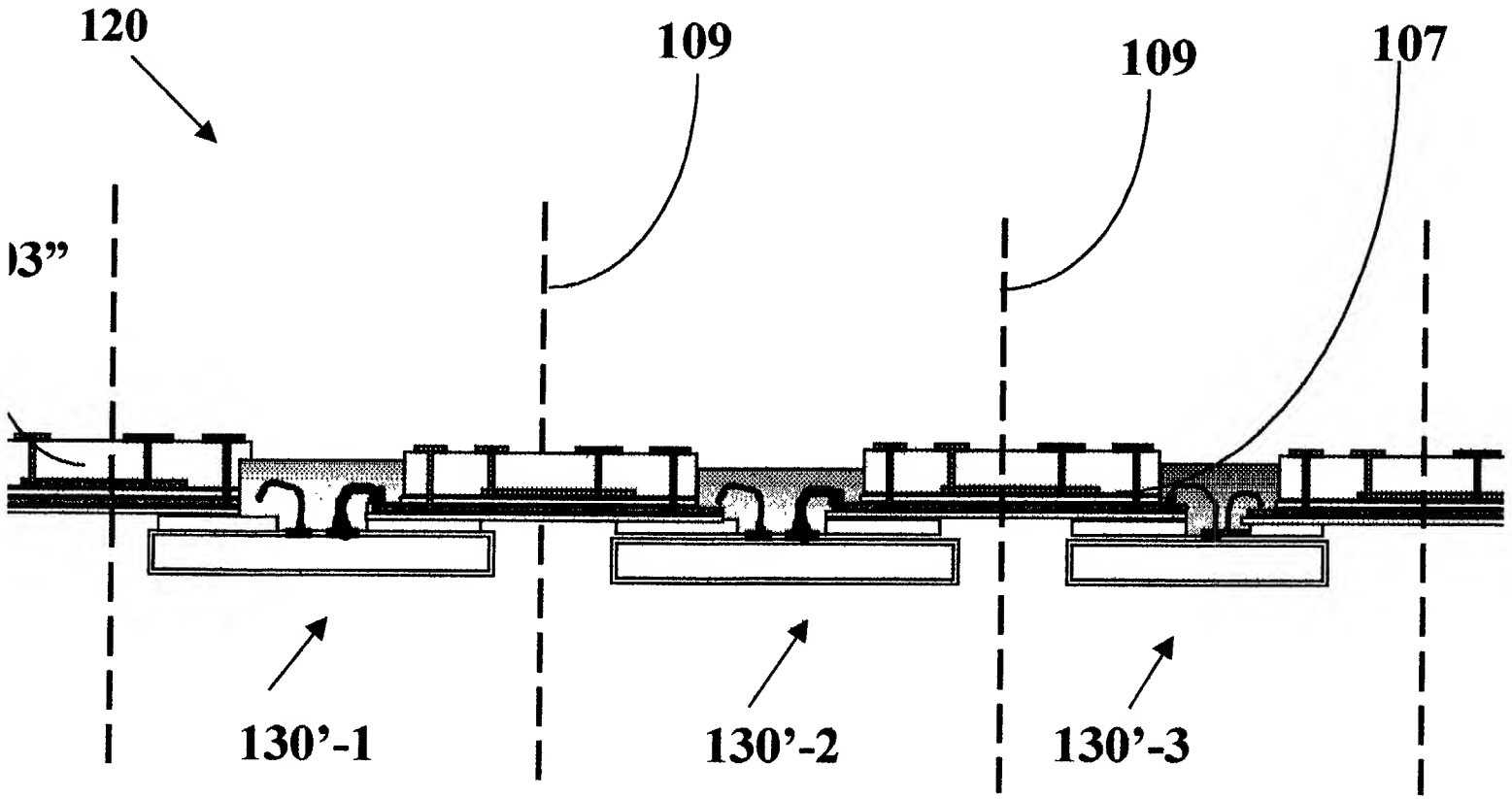


Fig.1B



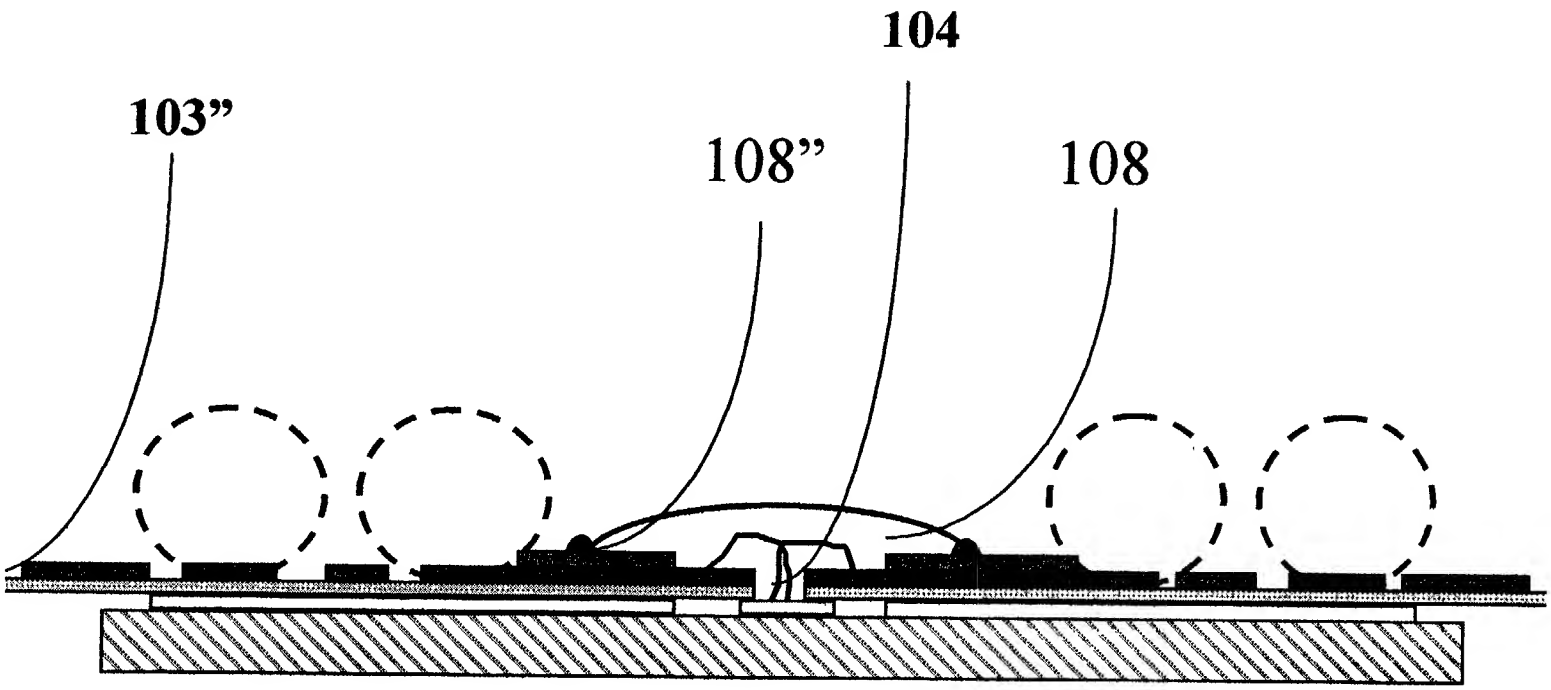


Fig. 1C

Fig. 1D

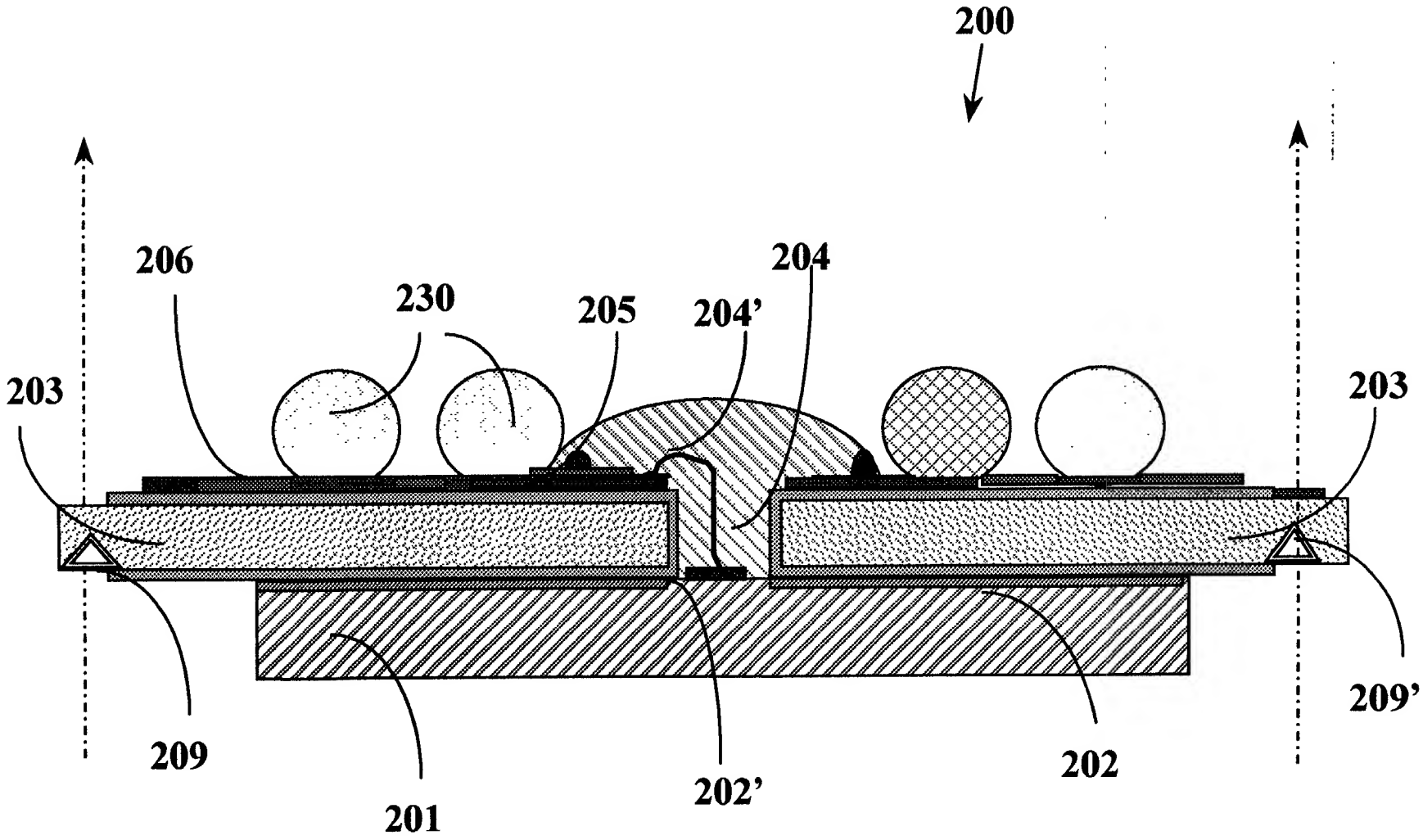


Fig. 2A

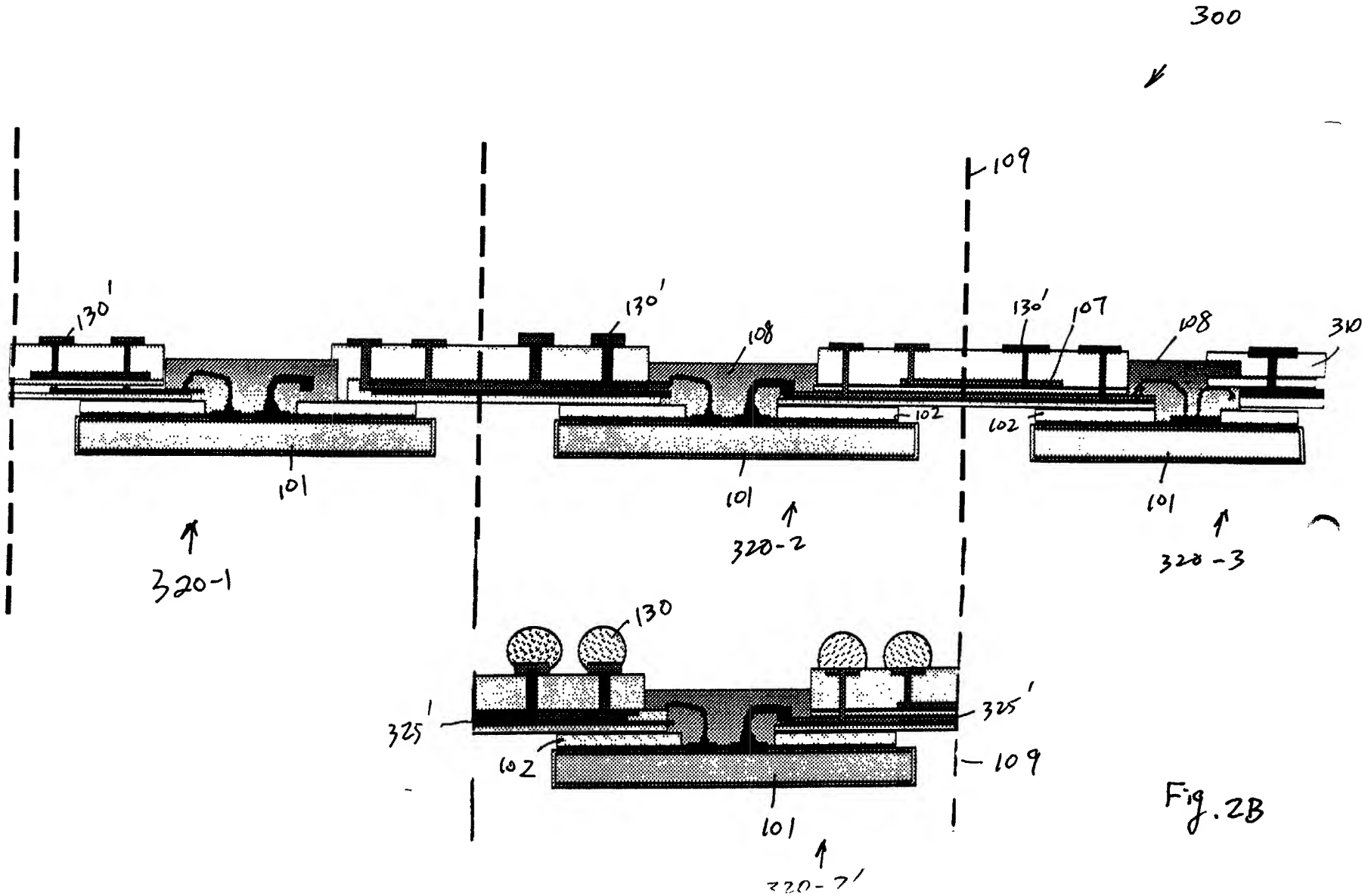


Fig. 2B

Fig. 2C

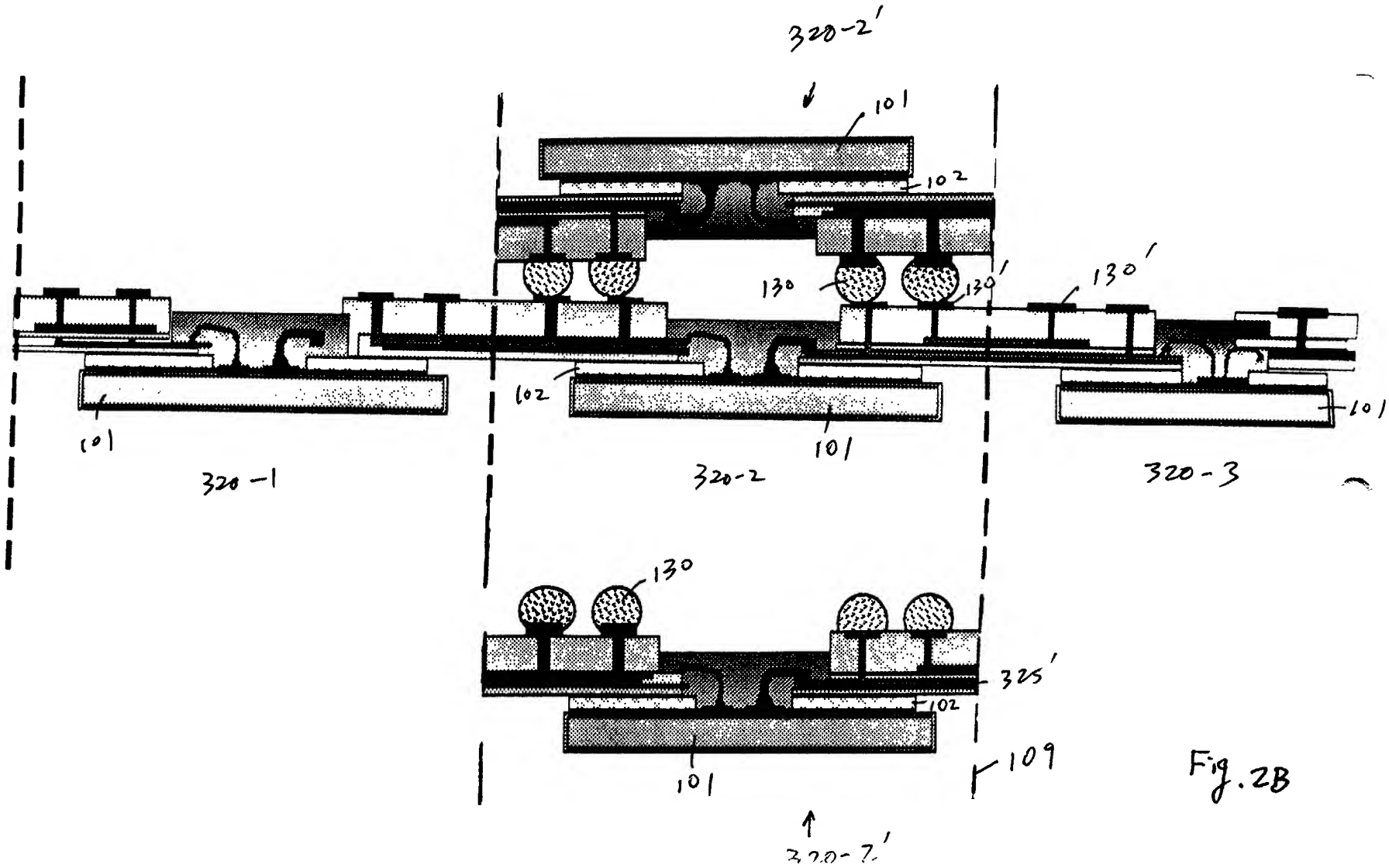


Fig. 2B

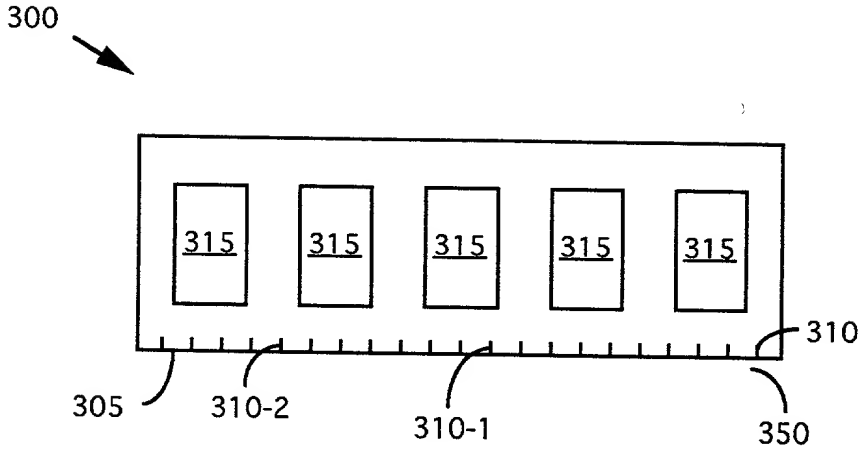

300
315
315
315
315
315
310
305
310-2
310-1
350

FIG. 3A

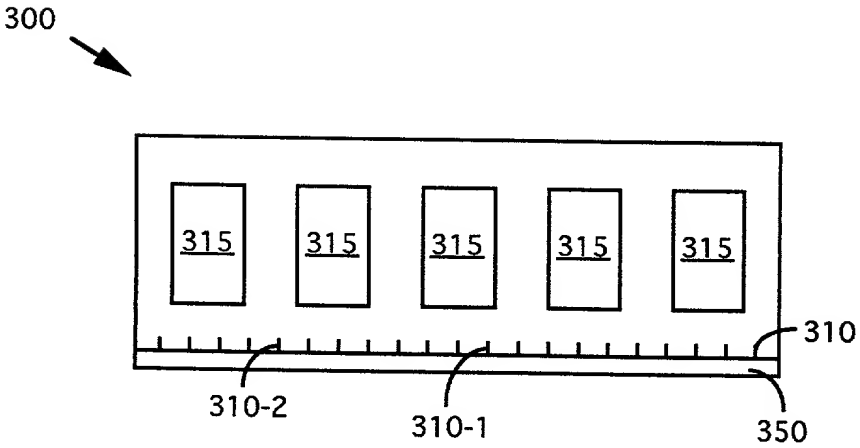

300
315
315
315
315
315
310
310-2
310-1
350

FIG. 3B

CONVENTIONAL MCM FLOW

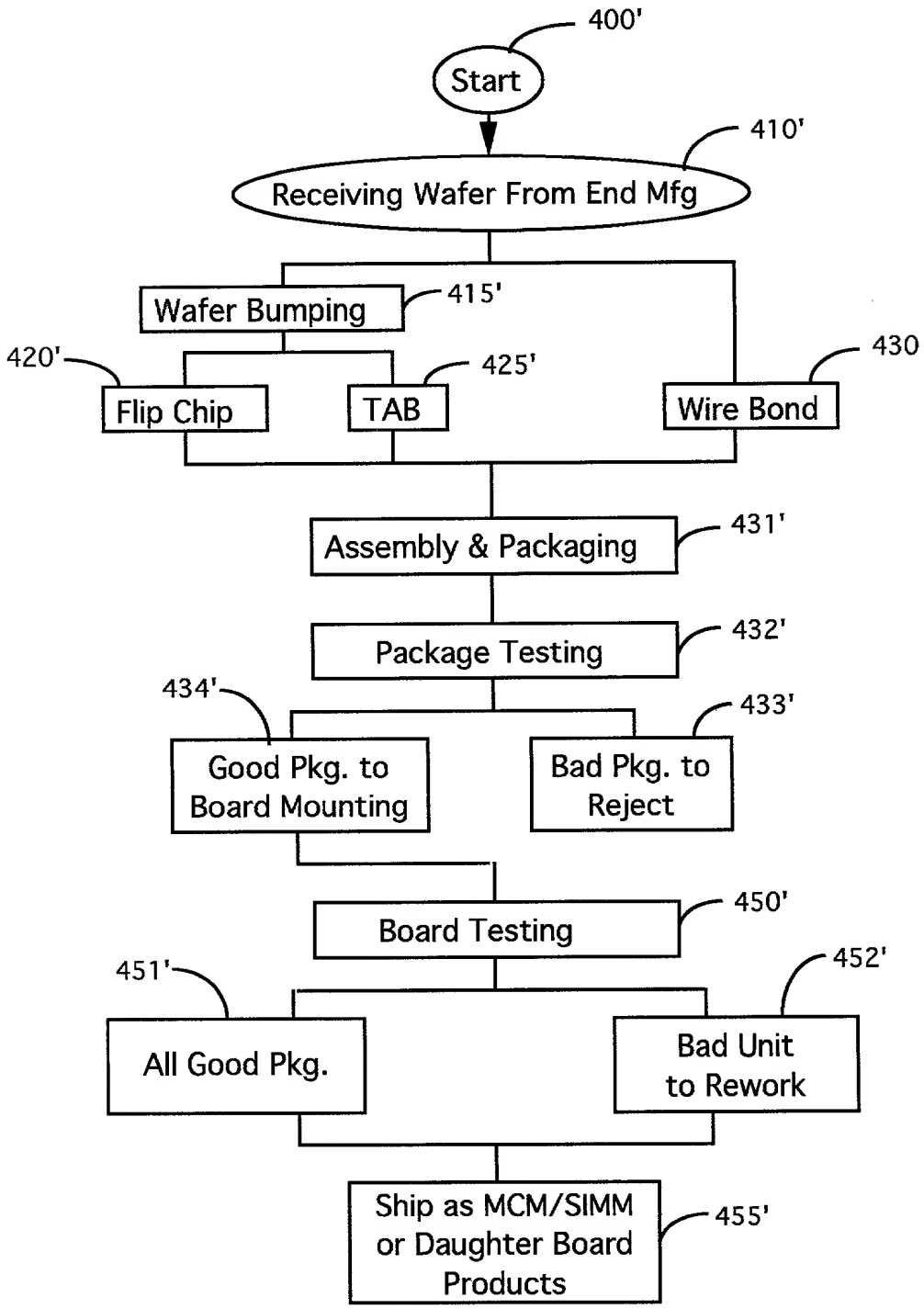


FIG. 4A

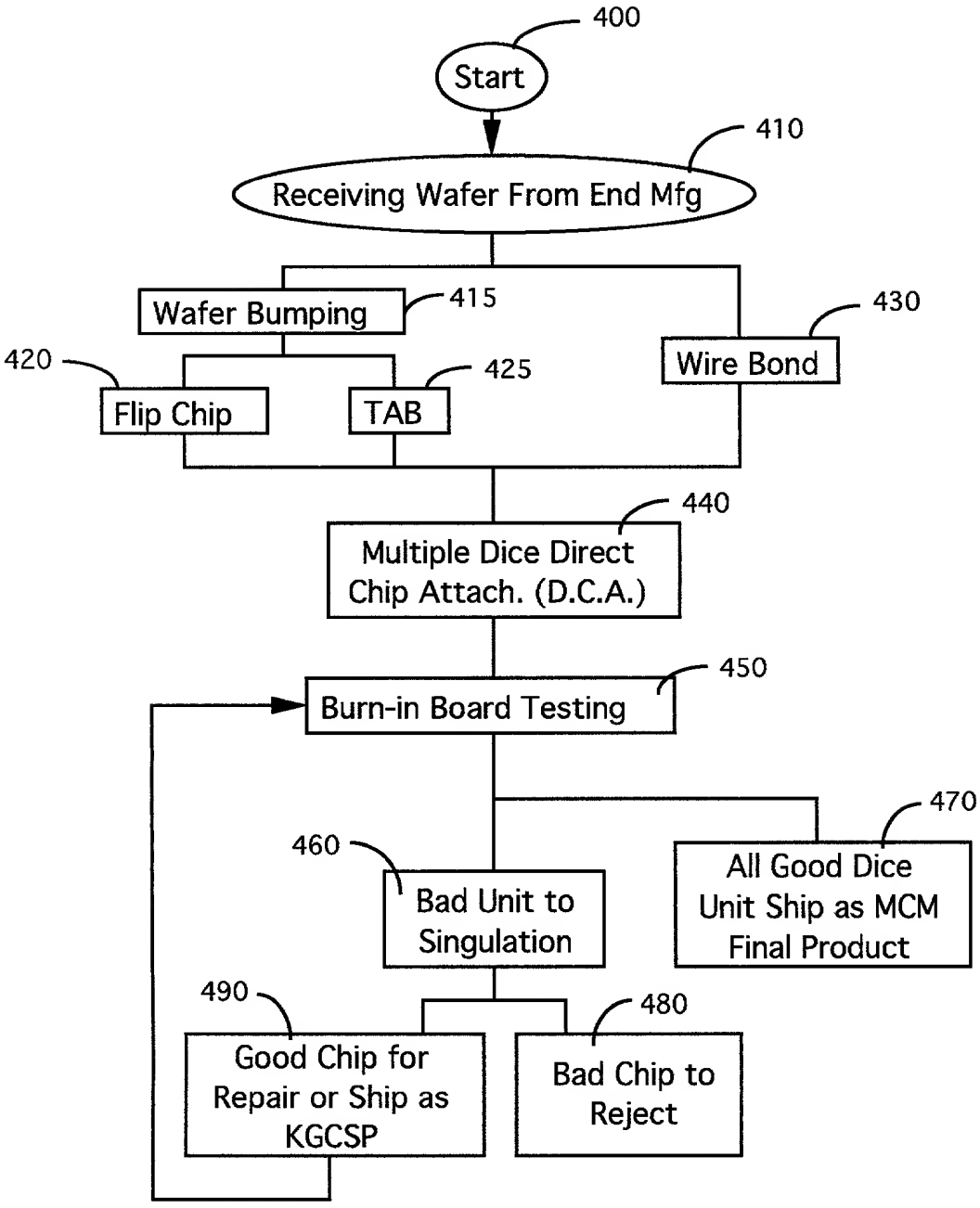

400
Start
410
Receiving Wafer From End Mfg
Wafer Bumping
415
430
420
Wire Bond
425
Flip Chip
TAB
440
Multiple Dice Direct
Chip Attach. (D.C.A.)
450
Burn-in Board Testing
470
460
Bad Unit to
Singulation
All Good Dice
Unit Ship as MCM
Final Product
490
480
Good Chip for
Repair or Ship as
KGCSP
Bad Chip to
Reject

FIG. 4B

Fig. 5

Very Stringent Requirements for SMT Packages

Package Qualification Tests with Level 3 Preconditioning

↓

10 X Temperature Cycle (-65 to +150 deg.C)

↓

Bake of 125 deg.C for 24 Hrs

↓

Temperature Humidity Soak (30 deg.C, 60%RH, 192Hrs)

↓

Vapor Phase (215 deg. C, 60 Sec., 3 Passes)

Thermal Shock Test	Temperature Cycle Test	AutoclaveTest	Temp.Humidity Bias
Liq. to Liq. -65 to +150 deg.C	Air to Air, -65 to + 150 deg.C	121 deg.C,	85 deg.C/85% RH
1000 Cycles	1,000 Cycles	100% RH	3.3 Volts
		15 PSIG	1008 Hrs.
		96 Hrs	

These requirements will not applied on edge connected sub-system such as SIMM/DIMM, PCMCIA or Slot 2 formats.

Docket No.PTLIN-9801

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Title: SUBSTRATE ON CHIP (SOC) MULTIPLE-CHIP MODULE (MCM) WITH CHIP-SIZE-PACKAGE (CSP) READY CONFIGURATION

the specification of which (check one)
_X_ is attached hereto.
__ was filed on_____as Application Serial No._____and was amended on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
			__ Yes __ No
(Number)	(Country)	(Day/Month/Year Filed)	

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

60/087,604	June 1, 1998	Pending
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Bo-In Lin(#33,948)

Send correspondence to: 13445 Mandoli Drive, Los Altos Hills, CA 94022

Direct Telephone Calls to: (name and telephone number)Bo-In Lin, (650) 949-0418 (Tel) 949-4118(Fax)

Docket No ETLIN-9801

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Full name of sole or first inventor: Paul T. Lin

Inventor's signature: Paul T. Lin Date: 5/18/99

Residence: 673 Hillcrest Terrace
Fremont, California 94539

Citizenship: United States of America

Post office address: 673 Hillcrest Terrace
Fremont, California 94539

Full name of second joint-inventor:

Inventor's signature: Date:

Residence:

Citizenship:

Post office address:

Full name of third joint-inventor:

Inventor's signature: Date:

Residence:

Citizenship:

Post office address:

Full name of fourth joint-inventor:

Inventor's signature: Date:

Residence:

Citizenship:

Post office address: